

REMARKS

This Amendment responds to the Office Action dated February 9, 2001 in which the Examiner rejected claims 1-6 under 35 U.S.C. §103.

As indicated above, minor informalities in the abstract and specification have been corrected. In particular, typographical errors have been corrected. It is respectfully requested that the Examiner approves the corrections.

Concurrently filed with this Amendment is a copy of the priority document. It is respectfully requested that the Examiner acknowledges the priority document.

Claims 1 and 6 claim a MOS transistor and a method of controlling a threshold voltage of a MOS transistor by applying a voltage of a first polarity to a substrate for inducing charges of a second polarity over a composition surface of a surrounded (or body) region. Thus, by controlling the threshold voltage in accordance with a body bias, as claimed in claims 1 and 6, the claimed invention provides a MOS transistor and method thereof which are capable of operating a circuit at a high speed while reducing power consumption. The prior art does not show, teach or suggest inducing charges of a second polarity over a composition surface of a surrounded (or body) region as claimed in claims 1 and 6.

Applicants respectfully traverse the Examiner's statement that a EIB is a MOS or junction, adapted for biasing the voltage of a substrate relative to the body. Applicants respectfully submit that a EIB is generally understood as a device not only biasing the voltage of the substrate, but also accumulating or inverting the interface between the SOI and the buried oxide.

Furthermore, Applicants respectfully traverse the Examiner's statement that a VT-MOS is a EIB-MOS. In particular, a VT-MOS is a conventional EIB-MOS.

Claims 1, 2 and 4-6 were rejected under 35 U.S.C. §103 as being unpatentable over *Burr* (U.S. Patent No. 6,100,567).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to the claims and allows the claims to issue.

Burr appears to disclose a fully depleted silicon-on-insulator (SOI) device which includes an intrinsic channel region and a mechanism for tuning the threshold voltage thereof. (col. 1, lines 9-12) A "fully depleted" SOI device is shown in FIG. 3. Here, the device is configured such that the depletion regions 328 extend completely down to the interface with the oxide layer 308. The structure is otherwise similar to that of the partially depleted device, and includes an nfet 302 having source and drain n-regions 312 and 314, a p-type channel region 316, and a gate 318, and a pfet 304 having source and drain p-regions 320 and 322, an n-type channel region 324, and a gate 326. The substrate 310 is tied to a fixed potential such as ground. (col. 1, lines 48-59) Another configuration that has been proposed is shown in FIG. 5. Here, a first buried back gate p+ well 540 is formed within a p- substrate 510 beneath the nfet 518 (having n-type source and drain regions 512 and 514, a p-type channel region 516, and a gate 518), and a second buried

back gate n+ well 542 is formed within the p- substrate beneath the pfet 504 (having p-type source and drains regions 520 and 522, an n-type channel region 524, and a gate 526). By providing separate contacts 544 and 546 in the conductive regions 540 and 542, respectively, separate bias potentials can be applied to the nfet 502 and pfet 504, thereby tuning the threshold voltage of each device. (col. 2, lines 46-57)

Thus, *Burr* merely discloses a device having a depletion region 328 which extends completely down to the interface with the oxide layer 308. Nothing in *Burr* shows, teaches or suggests a surrounded or body region including a depletion layer as claimed in claims 1 and 6 and new claims 7 and 12. Rather, *Burr* merely discloses an entire depletion region 328. (i.e. no depletion layer is found within the surrounded or body region). In particular, *Burr* merely discloses the prior art shown in Figure 4 and discussed on page 4 lines 6-12 of the specification. *Burr* discloses a threshold voltage which is controlled in accordance with the substrate bias (V_{sub}). However, as claimed in claims 1 and 6, the threshold voltage is controlled in accordance with the body bias (V_{body}) in which the substrate is applied with a voltage of a first polarity for inducing charges of a second polarity over a composition surface of the surrounded (or body) region.

Furthermore, Applicants respectfully traverse the Examiner's statement it would be obvious that a FET would include a composition surface in the depletion layer in contact with the insulating layer in which charges of a second polarity are induced. No such feature is shown, taught or suggested by *Burr*. Furthermore, since the depletion region 328 is depleted, the bias is non-variable. In other words, nothing in *Burr* shows, teaches or suggests inducing charges of a second polarity over a composition surface of a

surrounded or body region. Additionally, *Burr* merely discloses a depletion region 328 which extends completely down to the interface of the oxide layer. Thus, the state of the SOI back interface of *Burr* is depletion while in the present invention is inversion or accumulation. Furthermore, the substrate bias (V_{sub}) of *Burr* is variable whereas in the claimed invention the substrate bias is constant. Furthermore, the body bias (V_{body}) in *Burr* is non-variable because the body is depleted (depletion region 328). However, the body bias in the claimed invention is variable since the surrounded region or body region includes a depletion layer.

Since *Burr* is directed to controlling a threshold voltage based upon a substrate bias and not based upon a surrounded region (or body bias) as claimed in claims 1 and 6, it is respectfully requested that the Examiner withdraws the rejection to claims 1 and 6 and allows new claims 7-12.

Claims 2 and 4-5 depend from claim 1 and recite additional features. It is respectfully submitted that claims 2 and 4-5 would not have been obvious within the meaning of 35 U.S.C. §103 over *Burr* at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claims 2 and 4-5 under 35 U.S.C. §103.

Claim 3 was rejected under 35 U.S.C. §103 as being unpatentable over *Burr* in view of *Warashina et al.* (U.S. Patent No. 5,698,885).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claim has been reviewed in light of the Office Action, and for reasons

which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection to the claim and allows the claim to issue.

As discussed above, nothing in *Burr* shows, teaches or suggests the primary features of the claimed invention. Therefore, it is respectfully submitted that secondary reference will not overcome the deficiencies in the primary reference. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claim 3 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our
Deposit Account No. 02-4800.

Respectfully submitted,

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Marked-up Copy of Abstract

A MOS transistor with a controlled threshold voltage [comprises] includes a SOI which includes a substrate composed of a semi-conducting material, a single crystal layer composed of a semi-conducting material and an insulating layer interposed between the substrate and the single crystal layer. The single crystal layer is formed therein with a source region, a drain region and a surrounded region surrounded by the source region and the drain region. The surrounded region includes a depletion layer having a composition surface which is in contact with the insulating layer. The MOS transistor comprises an EIB-MOS transistor of which the substrate is adapted to be applied with a voltage of a first polarity for inducing charges of a second polarity over the composition surface of the surrounded region.

Marked-up Copy of Specification

Paragraph Bridging Pages 1 and 2

Normally, the threshold voltage is approximately constant while the transistor is turned on and off, however, it is possible to [controlling] control the threshold voltage by changing a substrate voltage of the MOS transistor. That is, the threshold voltage shift ΔV_{th} is expressed according to the following equation.

$$\Delta V_{th} = -\gamma V_{bs} \quad (1)$$

wherein γ is a body effect factor of the MOS transistor. Therefore, one way to compromise the fast operation and the reduction of the power consumption of the MOS transistor is that the threshold voltage is lowered when the MOS transistor is turned on and [is risen] risen when the MOS transistor is turned off by changing the substrate voltage of the MOS transistor.

Page 2, Paragraph Beginning at Line 6

In case of a VT MOS transistor composed by using the VT MOS technique, the threshold voltage of the VT MOS transistor is controlled by a whole of a chip in which the VT MOS transistor is provided. In this case, a first voltage is applied to a substrate of the VT MOS transistor in the active mode, and a second voltage smaller than the first voltage is applied to the substrate in the standby mode, thereby, the threshold voltage [is risen] risen.

Marked-up Copy of Specification

Page 2, Paragraph Beginning at Line 12

On the other hand, a DTMOS transistor such as a n type DTMOS transistor shown in Fig. 1 composed by using the DTMOS technique comprises a SOI 4 which includes a substrate 1 composed of a p type semiconducting material (e.g. silicon), a single crystal layer 2 composed of a semiconducting material (e.g. silicon) and an insulating layer 3 (e.g. silicon dioxide layer) interposed between the substrate 1 and the single crystal layer 2. The single crystal layer 2 is formed therein with [an] a n type source region 5, a n type drain region 6 and a p type body 7 surrounded by the source region 5 and the drain region 6. Further, a gate electrode 9 deposited on the body 7 through a gate oxide 8 is electrically connected to the body 7 through a wire 10 so that the threshold voltage of the DTMOS transistor is controlled. In other words, the threshold voltage is always lowered when the DTMOS transistor is turned on, and it [is] always [risen] risen when it is turned off.

Page 3, Paragraph Beginning at Line 11

With reference to the equation (1), in order to control the threshold voltage effectively, it is preferable to make the body effect factor γ high. However, in general, it is necessary to [rise] raise an impurity concentration of the MOS transistor in order to make the body effect factor of the MOS transistor high. As a result, the threshold voltage itself rises, and the fast operation of the MOS transistor is degraded. In such a circumstance, an optimization of the body effect factor γ has not been performed so far, and the body effect factor γ is normally about 0. 1 to 0. 3.

Marked-up Copy of Specification

Paragraph Bridging Pages 3 and 4

Wherein t_{fox1} is a thickness of a gate oxide 15 interposed between the substrate 13 and a gate electrode [15] 14, and 1_d is a depth of a depletion layer formed directly below the gate oxide 15. Therefore, it is necessary to [rise] raise the impurity concentration and lower the depth 1_d in order to make the body effect factors γ high. However, the threshold voltage becomes high if the impurity concentration becomes high, as described. This situation holds true in case of a partially depleted SOI MOS transistor.